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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,795	09/29/2003	Takayuki Gyohten	67161-108	1492

7590 07/25/2005

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/671,795	GYOHTEN ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Examiner took notice of the remarks and amendments made by applicant filed on 5/20/05.

2. A second non-final rejection is applied to the pending claims using newly cited reference.

Response to Amendment

3. This office action is in response to Amendment filed on 5/20/05.

Claim 1, 3, 4, 6, and 9 are amended.

Claim 2 is canceled.

4. Claims 8 and 3-10 are pending.

Claim Rejections - 35 USC ∋ 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 3-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi, Pat. No. 6295240.

With regard to claim 1, Choi discloses a memory cell storing data (fig. 2, 21); a pair of bit lines (fig. 2, DB and /DB) connected to said memory cell (fig. 2, 21); a sense amplifier (fig. 2, 22) provided corresponding to the pair of bit lines and activated in

response to a sense amplifier activation signal; a pair of I/O lines (fig. 2, DB and /DB) lines transmitting said data input/output to/from said memory cell via said pair of bit lines; and a connection gate circuit (fig. 2, 23, 24) provided between said bit lines and said pair of I/O lines and electrically connecting said pair of bit lines to said pair of I/O lines when said sense amplifier activation signal and a column selection signal selecting said pair of bit lines are both activated (col. 2, line 23-34); wherein said connection gate circuit (fig. 2, 23, 24) includes first (fig. 2, 24) and second gates (fig. 2, 23) connected in series between said pair of bit lines and said pair of I/O lines, said first gate conducts in response to said sense amplifier activation signal (fig. 2, SA_STROBE) and said second gate (fig. 2, 23) conducts in response to said column selection signal (fig. 2, COLUMN_SELECT) (Col. 2, line 350-59) (also with regard to claim 4 a d 5).

With regard to claim 6, Choi discloses a memory cell storing data (fig. 2, 21); a pair of bit lines (fig. 2, DB and /DB) connected to said memory cell (fig. 2, 21); a sense amplifier (fig. 2, 22) provided corresponding to the pair of bit lines and activated in response to a sense amplifier activation signal; a pair of I/O lines (fig. 2, DB and /DB) lines transmitting said data input/output to/from said memory cell via said pair of bit lines; and a connection gate circuit (fig. 2, 23, 24) provided between said bit lines and said pair of I/O lines and electrically connecting said pair of bit lines to said pair of I/O lines when said sense amplifier activation signal and a column selection signal selecting said pair of bit lines are both activated (col. 2, line 23-34); logic gate circuit (fig. 2, ND21`, ND22, 25) activating its output signal when said sense amplifier activation signal (fig. 2, SA_STROBE) and said column selection signal (fig. 2, COLUMN_SELECT) are

activated; wherein said connection gate circuit (fig. 2, 23, 24) includes a gate conducting in response to said output signal (fig. 2, SW_CNT2, SW_CNT1) from said logic gate circuit (fig. 2, ND21, ND22, 25) (also with regard to claim 7 and 8).

Claim Rejections - 35 USC ∋ 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi, Pat. No. 6295240 in view of Ikeda, Pat. No. 6314045 (previously cited).

With regard to claim 3, as applied in prior rejection Choi disclose disclosed all claimed subject matter an equalization circuit equalizing potentials of a pair of nodes connecting said first gate with said second gate of the connection gate circuit. However, Ikeda discloses an equalization circuit (fig. 8, PE) for equalizing the potentials of a pair of bit line (col. 7, line 44-61) of the memory device. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate the equalization circuit of Ikeda's into Choi's for the purpose of to bring the bit lines connected by the first and second gate to an equalized potential.

Allowable Subject Matter

7. Claim 9 and 10 are allowed.

The prior art of record does disclosed in combination with other features, the limitation of said connection gate further includes another gate conducting in response to a write mask signal, and said gate and said another gate are connected in series between said pair of bit lines and said pair of I/O lines.

Conclusion

8. When responding to the office action, Applicants= are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

July 2005

CONNIE C. YOHA
PRIMARY EXAMINER